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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,166	09/24/2003	Toshio Kimura	1035-473	4031

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,166	KIMURA ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 4 is objected to because of the following informalities: it redundantly recites "wherein" (ln 1, 2). Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 6,661,100) in view of Hayasaka (US 6,809,421).

3. Regarding claim 1, Anderson discloses (Fig 2) a semiconductor device, comprising:

a plurality of spaced apart electrodes (connections 205; col 4 ln 2) with equal cross-sectional areas on a semiconductor chip (200; col 3 ln 65),

a first number of the plurality of electrodes being electrically connected to one another to form a first high-current electrode (210) in communication with a power supply (VDD; col 4 ln 10-12), a second number of the plurality of electrodes being electrically connected to one another to form a second high-current electrode (220) in

communication with ground (GND; col 4 ln 4-6), and wherein a particular signal-routing electrode (205) is formed of only one of the plurality of through electrodes; and

wherein at least one of the first number and the second number is two or greater (the number connected in both 210 and 220 is greater than two), so that at least one of the first high-current electrode and the second high-current electrode is made up of at least two of the electrodes which are electrically connected to one another.

4. Further regarding claim 1, Anderson differs from the claimed invention only in not disclosing the electrodes are "through" electrodes "linking a front surface of the chip to a back surface of the chip". Hayasaka discloses (Fig 4) through electrodes (4; col 10 ln 30-34). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson by forming at least the peripheral electrodes (205, 212, 220) to be through electrodes, as taught by Hayasaka; at least to allow stacking and connecting more than two chips (Hayasaka: col 10 ln 46-54).

5. Regarding claim 2, Anderson discloses at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip (inherent, this must be true, or the device of Anderson would not function).

6. Regarding claim 3, Anderson as modified by Hayasaka differs from the claimed invention only in not expressly disclosing "non-contact" through electrodes. Hayasaka discloses through electrodes used only for heat radiation (col 11 ln 15-16). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson such that at least one type of the through electrodes is

non-contact through electrodes not electrically connected to that semiconductor chip, as suggested by Hayasaka; at least to radiate heat (Hayasaka: col 11 ln 16).

7. Regarding claim 4, Anderson as modified by Hayasaka discloses both of the first number and the second number is two or greater (Anderson: Fig 2), so that each of the first (210) and second (220) high-current through electrodes is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode (205) is made up of only one of the through electrodes.

8. Regarding claim 5, Anderson as modified by Hayasaka discloses multiple stacked semiconductor chips (Hayasaka: col 10 ln 46-54), each of the semiconductor chips including a semiconductor device according to claim 1 (Hayasaka: Fig 4).

9. Regarding claim 6, Anderson discloses (Fig 2) a chip-stack semiconductor device, comprising:

a plurality of stacked semiconductor chips (Fig 3A, 3C: 310, 340; col 4 ln 35-41), each of the semiconductor chips including a plurality of electrodes (205; col 4 ln 1-2) with equal cross-sectional areas,

wherein at least one of a first high-current electrode (210) connected to a power supply (VDD; col 4 ln 10-12) and a second high-current electrode (220) connected to ground (GND; col 4 ln 4-6) is made up of at least two electrodes which are electrically connected to one another (col 4 ln 3-4), whereas a signal-routing electrode (205) is made up of only one of the electrodes, and

at least one of the electrodes is a contact type electrode which is electrically connected to the semiconductor chip in which it is formed (inherent, this must be true, or the device of Anderson would not function).

10. Further regarding claim 6, Anderson differs from the claimed invention only in not disclosing the electrodes are "through" electrodes "linking a front surface of the chip to a back surface of the chip". Hayasaka discloses (Fig 4) through electrodes (4; col 10 ln 30-34). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson by forming at least the peripheral electrodes (205, 212, 220) to be through electrodes, as taught by Hayasaka; at least to allow stacking and connecting more than two chips (Hayasaka: col 10 ln 46-54).

11. Regarding claim 7, , Anderson discloses (Fig 2) a chip-stack semiconductor device, comprising:

a plurality of stacked semiconductor chips (Fig 3A, 3C: 310, 340; col 4 ln 35-41), each of the semiconductor chips including a plurality of electrodes (205; col 4 ln 1-2) with equal cross-sectional areas,

wherein at least one of a first high-current electrode (210) connected to a power supply (VDD; col 4 ln 10-12) and a second high-current electrode (220) connected to ground (GND; col 4 ln 4-6) is made up of at least two electrodes which are electrically connected to one another (col 4 ln 3-4), whereas a signal-routing electrode (205) is made up of only one of the electrodes.

12. Further regarding claim 7, Anderson differs from the claimed invention only in not disclosing the electrodes are "through" electrodes "linking a front surface of the chip to a back surface of the chip". Hayasaka discloses (Fig 4) through electrodes (4; col 10 ln 30-34). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson by forming at least the peripheral electrodes (205, 212, 220) to be through electrodes, as taught by Hayasaka; at least to allow stacking and connecting more than two chips (Hayasaka: col 10 ln 46-54).

13. Further regarding claim 7, Anderson as modified by Hayasaka differs from the claimed invention only in not expressly disclosing "non-contact" through electrodes. Hayasaka discloses through electrodes used only for heat radiation (col 11 ln 15-16). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson such that at least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed, as suggested by Hayasaka; at least to radiate heat (Hayasaka: col 11 ln 16).

14. Regarding claim 8, Anderson discloses (Fig 2) a chip-stack semiconductor device, comprising multiple stacked semiconductor chips (Fig 3A, 3C: 310, 340; col 4 ln 35-41), each of the semiconductor chips including a number of electrodes (205; col 4 ln 1-2) with equal cross-sectional areas,

wherein a number of adjacent connected ones of the electrodes which are connected to either a ground terminal (220: GND; col 4 ln 4-6) or a power supply

terminal (210: VDD; col 4 ln 10-12) of that semiconductor chip (200) is greater than a number (0) of adjacent connected ones of the electrodes (205) which are connected to a particular signal terminal thereof.

15. Further regarding claim 8, Anderson differs from the claimed invention only in not disclosing the electrodes are "through" electrodes "linking a front surface of the chip to a back surface of the chip". Hayasaka discloses (Fig 4) through electrodes (4; col 10 ln 30-34). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson by forming at least the peripheral electrodes (205, 212, 220) to be through electrodes, as taught by Hayasaka; at least to allow stacking and connecting more than two chips (Hayasaka: col 10 ln 46-54).

16. Further regarding claim 8, Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18), but differs from the claimed invention only in not expressly disclosing determining the number of the through electrodes. It is well known that a larger total conductor cross-section results in a lower impedance. It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the number of the through electrodes be determined in accordance with a magnitude of an electric current to be conducted therethrough; at least to reduce impedance.

17. Regarding claims 9-12, Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18), but differs from the claimed invention only in not expressly disclosing the number of through electrodes used in connecting different numbers of

chips. It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance. Anderson as modified by Hayasaka discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent in the structure of Hayasaka Fig 4). It would have been obvious to a person having ordinary skill in the art at the time the invention was made that a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2; at least to reduce impedance.

18. Regarding claims 13-16, Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18), but differs from the claimed invention only in not expressly disclosing the number of through electrodes is increased with interconnect line length. It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance. It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is increased; at least to reduce impedance.

19. Regarding claims 17-20, Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18), but differs from the claimed invention only in not

expressly disclosing the number of through electrodes is increased with interconnect line length. It is well known that a total conductor cross-section is increased in proportion with an increasingly longer conduction path length to reduce impedance. It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the first and second number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips; at least to reduce impedance.

Response to Arguments

20. Applicant's arguments with respect to claims 1-20, filed 02/02/2006 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOA
04/10/2006

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